AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 0001 with the following amended paragraph:

The present invention is related to issued U.S. patent No. 7,289,369, ~~U.S. Application Serial No. _____ (Attorney Docket No. YOR20030364US1)~~ entitled "CLOCK GATED POWER SUPPLY NOISE COMPENSATION" to Phillip J. Restle, filed coincident herewith and assigned to the assignee of the present invention.

Please replace paragraph 0029 with the following amended paragraph:

As is also apparent from the supply noise characterization plot example of Figure 2A, typical noise events are relatively long, lasting several cycles and even many cycles. Once the relationship between the FO4 number reduction and supply line drop is determined, e.g., as described for the flow chart of Figure 2B, the present invention (e.g.,) can be used to accurately characterize supply noise, generating a plot similar to that of Figure 2A, e.g., using the logic stage counter 100 of Figure 1. Figure 2C shows an example of a flow chart 220 for generating a characterization plot by iteratively logging edges during such an event. In step 222 a logger count is initialized to point to the beginning or just before the beginning of the particular event. Then, in step 224 both the cycle counter and the chip are initialized to an initial state and started. Essentially, supply noise is characterized by repeatedly scanning through the particular event and logging tap contents at successive cycles during the scan. So in step 226 in the first pass, the contents of the capture register are collected after N cycles, near in time to the beginning of the particular on-chip switching noise event and, in step 226 the tap locations are logged. In step 228 the current logger count is checked to determine if the count is at or after the end of the event. Next, since the count is not at the end of the event, in step 130, the logger count is incremented and, returning to step 224, the chip is restarted from the same initial state and run for N+1 cycles, and in step 226 the tap

locations of the captured edges are logged. This is repeated for N+2 cycles, N+3 cycles, and etc., until in step 228, it is determined that the event has passed. The collected tap locations are converted to mV and the on-chip VDD level may be plotted against time (cycle number) to recover the waveform as in the example of Figure 2A. Further, once the relationship between supply noise and FO4 number reduction is ascertained, such noise can be mitigated as described in issued U.S. patent No. 7,289,369, ~~U.S. Application Serial No. _____ (Attorney Docket No. YOR20030364US1)~~ entitled "CLOCK GATED POWER SUPPLY NOISE COMPENSATION" to Phillip J. Restle, filed coincident herewith, assigned to the assignee of the present invention and incorporated herein by reference.